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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,340	03/26/2004	Pavel Horsky	BGC.003US (A2259-US)	8208

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EXAMINER	
NATALINI, JEFF WILLIAM	
ART UNIT	**PAPER NUMBER**
2858	

DATE MAILED: 04/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/810,340	HORSKY ET AL.	
	Examiner	Art Unit	
	Jeff Natalini	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Van Herzeele (EP 1102405- herein to be referred to as Herzeele).

In regard to claim 1, Herzeele discloses measuring a physical value (abstract), comprising during a clock cycle (fig 5, (clk input); uses sense means for measuring a parameter each clock cycle): forming an input signal (fig 5 (CPin, CNin)), a reference signal (Pref, Nref), and an offset signal (Poff, Noff), the input signal including a parasitic value and a useful measurement value (col 6 line 14-23; the output of the sensor, which contains a real differential signal and an offset voltage (parasitic value) that needs to be eliminated, is the input signal of the device for offset corection-ADCb), the signals being respectively associated with an input element (fig 5-SM), a reference element (reference resistors in fig 5 –SRSa) and a parasitic element (offset resistors in fig 5-SRSa) , all elements having a common driving signal (fig 5-Vexc), the parasitic value depending on the common driving signal (col 1 line 11-12); and deriving a relationship between the input signal, from which the parasitic value has been cancelled out (col 3 line 3-6), and the reference signal (this relationship is shown in fig 2), and from this relationship, determining a value relating to the physical value (abstract).

In regard to claim 2, Herzeele discloses wherein the input signal is a first voltage (col 5 line 56 – col 6 line 1).

In regard to claim 3, Herzeele discloses wherein the first voltage is obtained from a direct voltage drop over the sensing element (fig 5, it is seen CNin and CPin are obtained from the voltage drop across the top resistors respectively).

In regard to claims 4 and 5, Herzeele discloses wherein the reference signal is a second voltage (fig 5, Pref is the signal off of the top resistor of the resistor string SRSa, being supplied by a voltage Vexc; col 7 line 55 – col 8 line 1).

In regard to claims 6 and 7, Herzeele discloses wherein the reference signal is a voltage drop over the reference element which is a resistor (fig 5, Pref is the signal off of the top resistor (reference resistor) of the resistor string SRSa, being supplied by a voltage Vexc).

In regard to claims 8-10, Herzeele discloses wherein the offset signal is a third voltage (col 6 line 17-20).

In regard to claim 11, Herzeele discloses wherein the third voltage is obtained from a direct voltage drop over the parasitic element (fig 5- offset is obtained with the voltage drop from Poff connected to the top of the 3rd resistor of the resistor string (SRSa) to Noff connected to the bottom of the resistor string).

In regard to claim 12, Herzeele discloses wherein the physical value is a temperature or a pressure (abstract).

In regard to claim 13, Herzeele discloses means for measuring a physical value comprising

an analog-to-digital converter (fig 5 (ADCb)) with at least a first (input), a second (reference) and a third port (offset), each of the at least three ports being suitable for receiving an input signal from an element (abstract, receives signal from sensor), the analog-to-digital converter being suitable for evaluating the physical value (abstract) in one measurement cycle (fig 5, (clk input); uses sense means for measuring a parameter each clock cycle),

a sensing element (abstract first sentence), having a pre-defined characteristic parameter related to the physical value to be measured (col 1 line 31-33, the output voltage of the sensor is a function of the physical value, so there is a parameter in the sensing means causing the voltage to be a function of the physical value) being coupled to the first port for applying an input signal to said first port (fig 5 (SM) applies Pin and Nin into the analog to digital converter),

a reference element being coupled to the second port for applying a reference signal to the second port (Pref is applied to the A/D converter through the value of the top resistor of string SRSa),

an element corresponding to a parasitic value of the sensing element, being coupled to the third port for applying a parasitic value of the sensing element to the third port (Poff is applied through the value off the second resistor in resistor string SRSa),

means for deriving a relationship between the input signal, from which the parasitic value of sensing element has been cancelled out (col 3 line 3-6), and the

reference signal (this relationship is shown in fig 2); and means for deriving, from the relationship, a value relating to the physical value (abstract).

In regard to claim 14, Herzeele discloses wherein the reference element is in series with the sensing element (fig 5 (SM is in series with the element in SRSa where the reference signal is being drawn from)).

In regard to clams 15 and 16, Herzeele discloses wherein the element corresponding to a parasitic value of the sensing element is coupled in series with the sensing element (fig 5, SM in series with the part of SRSa where the offset (parasitic) signal is being drawn from).

In regard to claim 17, Herzeele discloses wherein the reference element is a reference resistor (fig 5, Pref is the signal off of the top resistor (reference resistor) of the resistor string SRSa, being supplied by a voltage Vexc).

In regard to claim 18, Herzeele discloses wherein the physical value is a temperature or a pressure (abstract).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Eryuret (US 5700090) teaches a temperature sensor that has a input and reference element that is input into a comparator before being supplied to a analog to digital converter, wherein the A/D converter has an input for a parasitic parameter to be eliminated from the sensed measurement for accurate temperature readings. Falik (US 6870357) teaches a method for measuring temperature of

semiconductor wafers that has an input and reference input and a correction factor to eliminate parasitic resistance. Fletcher (US 5655305), Strong (US 4217543), and Hayashi (US 3875503) contain pertinent art that was cited by applicant in specifications, but was not disclosed in an IDS.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Natalini whose telephone number is 571-272-2266. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lefkowitz can be reached on 571-272-2180. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeff Natalini

ANJAN DEB
PRIMARY EXAMINER